MBI5042 Application Note

(The article is suitable for the IC whose version code is B and datasheet version is VB.0X)

Forward

MBI5042 uses the embedded PWM signal to control grayscale output and LED current. In contrast to the conventional LED driver which uses an external PWM signal, MBI5042 has more outstanding behavior in grayscale performance and is suitable for LED full-color display.

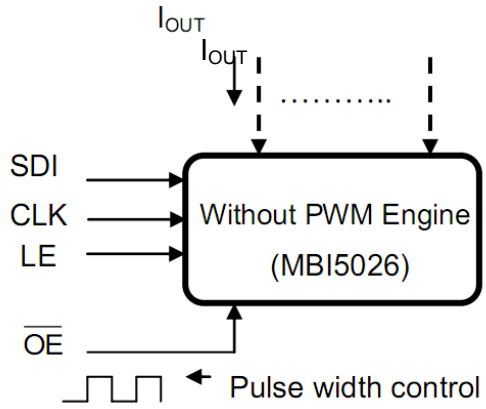

Figure 1. The traditional LED driver

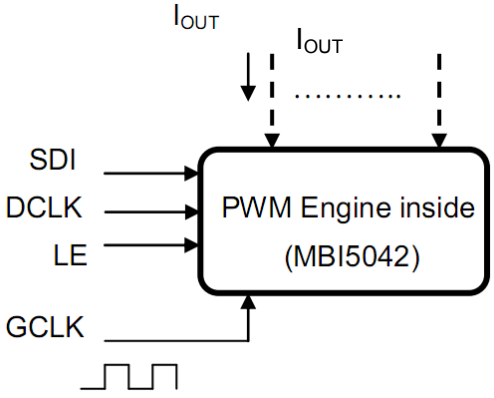

Figure 2. Embedded-PWM LED driver

Figure 1 shows the operation scheme of the traditional LED driver. It controls LED color gradation and brightness by sending variable pulse width signals (PWM) through $\overline{OE}$ pin. $\overline{OE}$ signal will suffer distortion and decay in long distance transmission, and furthermore causing a poor brightness control for LED while using more grayscale bits.

Figure 2 shows the scheme of PWM-embedded LED driver. The GCLK is used to trigger the internal PWM counter and output a PWM pulse to control the LED color gradation and brightness. Though the GCLK has the same problems in long distance transmission, but the distorted and decayed GCLK signal will not affect the LED brightness control while using more grayscale bits. Since GCLK is the trigger of PWM counter, the variable pulse width won't affect the internal PWM engine.

Besides, MBI5042 also features GCLK rising/falling edge trigger, 6-bit current gain adjustment and ghost reduction method. This article provides the application notices, such as the input method of image data and the setting of grayscale data. The detail operations are listed in the following chapters.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Section 1: Principle of Operations

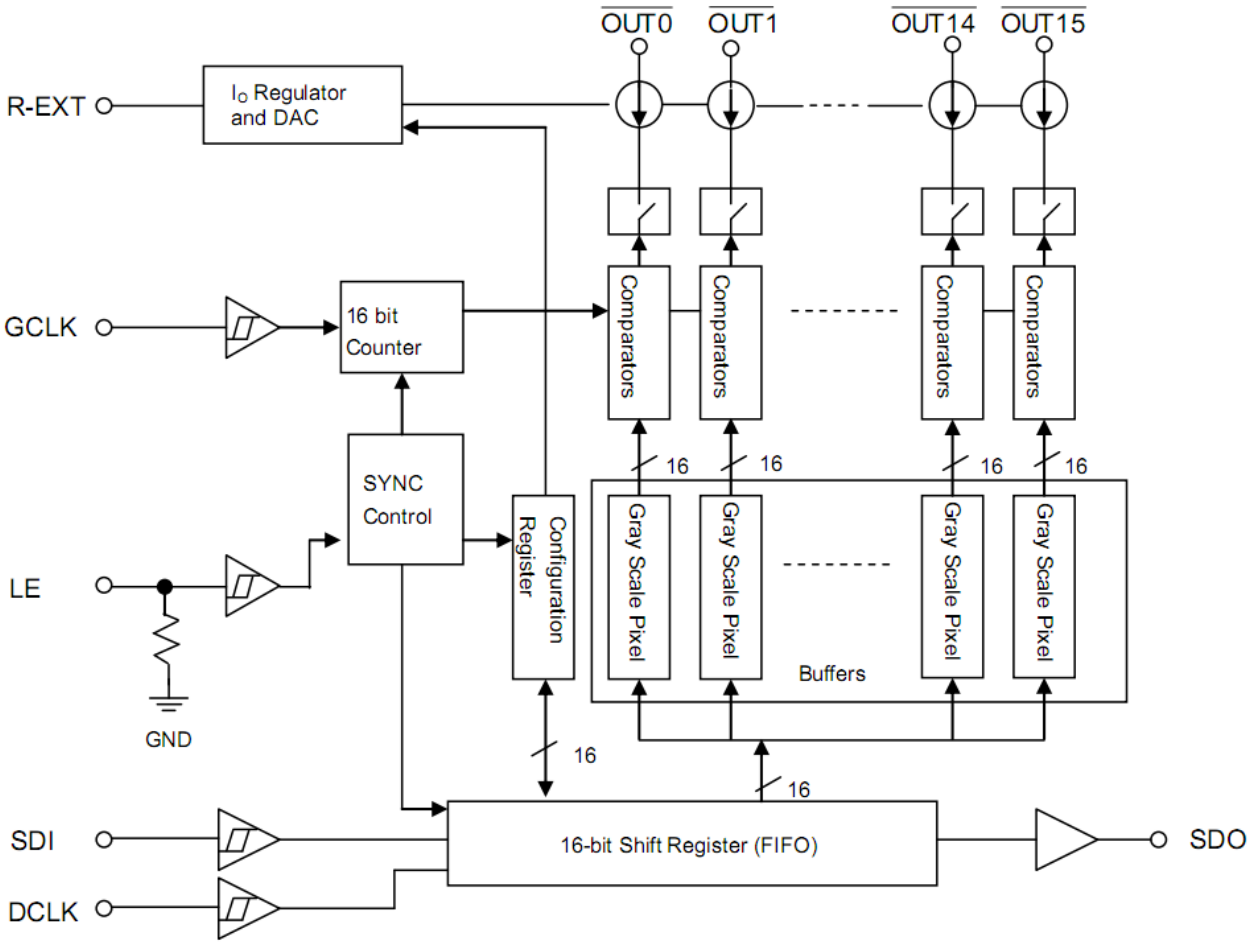

Figure 3. MBI5042 Block Diagram

Figure 3 shows the block diagram of MBI5042, the function of each pin is described as below.

Input Pins of Control Signal

DCLK → Data Clock Input pin

SDI → Grayscale Data Input pin

LE → The combination of LE and DCLK can be used to control command.

The grayscale data of MBI5042 is the combination of DCLK, SDI and LE. On the rising edge of DCLK, MBI5042 reads one bit data from SDI and inputs to the internal 16-bit shift register. The LE handles the “data latch” command of the internal 16-bit shift register.

Serial Data Output Pin (SDO)

SDO→ Serial Data Output pin. The SDO of first device is connected to the SDI of second device and so on. The grayscale data can be transmitted to next MBI5042.

PWM Counter Clock Input Pin (GCLK)

GCLK→ The frequency of GCLK determines the speed of internal PWM counter, and also the output frequency of $\overline{OUT0} \sim \overline{OUT15}$.

Current Setting Pin (R-EXT)

R-EXT→ Rext is used to connect an external resistor to set up the output current of all output channels.

LED Driver Output Pin

$\overline{OUT0} \sim \overline{OUT15}$ → Output Channel Pin. In generally, every channel can connect to one or more LEDs which depend on the circuit design.

Section 2: The Basic Settings of Grayscale

Sixteen output channels of MBI5042 can receive different grayscale data individually. The grayscale data length of each channel is 16 bits, so the data length of 16 channels is 256 bits (16 bits X 16 channels =256 bits). The sequence of input data is $\overline{OUT15}$ → $\overline{OUT14}$ →…→ $\overline{OUT0}$.

The sequence of grayscale data is from the MSB first, loading the data from channel 15 to channel 0. The length of shift register is 16 bits, such that to ensure the second MBI5042 can receive exactly 16bits grayscale data via the first MBI5042. Then, the LE signal latches the grayscale data of each channel into data buffers.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

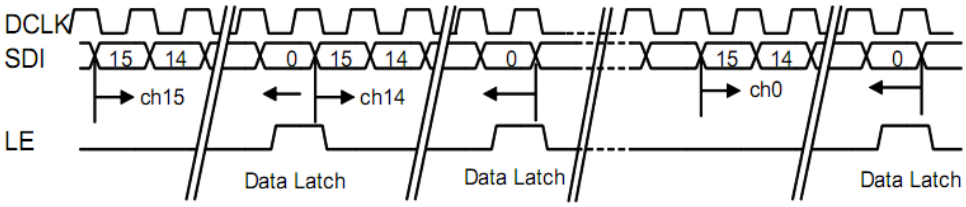

Figure 4. 16-bit grayscale data input and data latch command

After grayscale data of 16-channels are latched to data buffers, it needs a “global latch” command to update the frame data. A notice must be taken, the GCLK must be stopped before the global latch, and the interval between LE falling edge and GCLK rising edge must longer than 20ns.

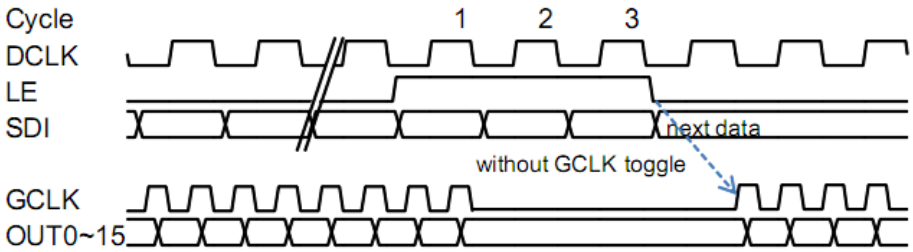

Figure 5. Global latch command

Section 3: The Grayscale Data Setting when Multi Driver Cascaded

If there are Npcs of MBI5042 in cascaded, as figure 6 shows, then the data length of each “data latch” is 16 x N bits.

For one MBI5042, each 16 bits grayscale data needs a data latch.

For two MBI5042 in cascaded, each 32 bits grayscale data needs a data latch.

For three MBI5042 in cascaded, each 48 bits grayscale data needs a data latch, and so on.

No matter how many MBI5042 are cascaded, the latch signals are the same. As figure 7 shows, the latch signal must be arrested until all the grayscale data has been inputted.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

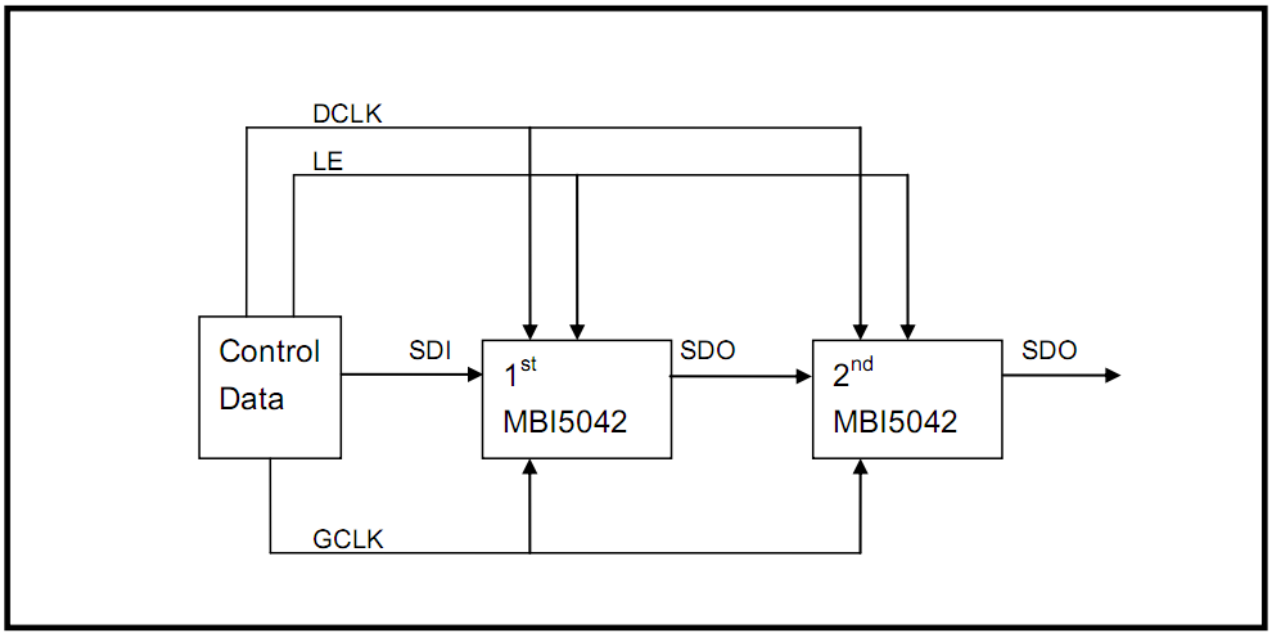

Figure 6. 2pcs of MBI5042 in cascaded

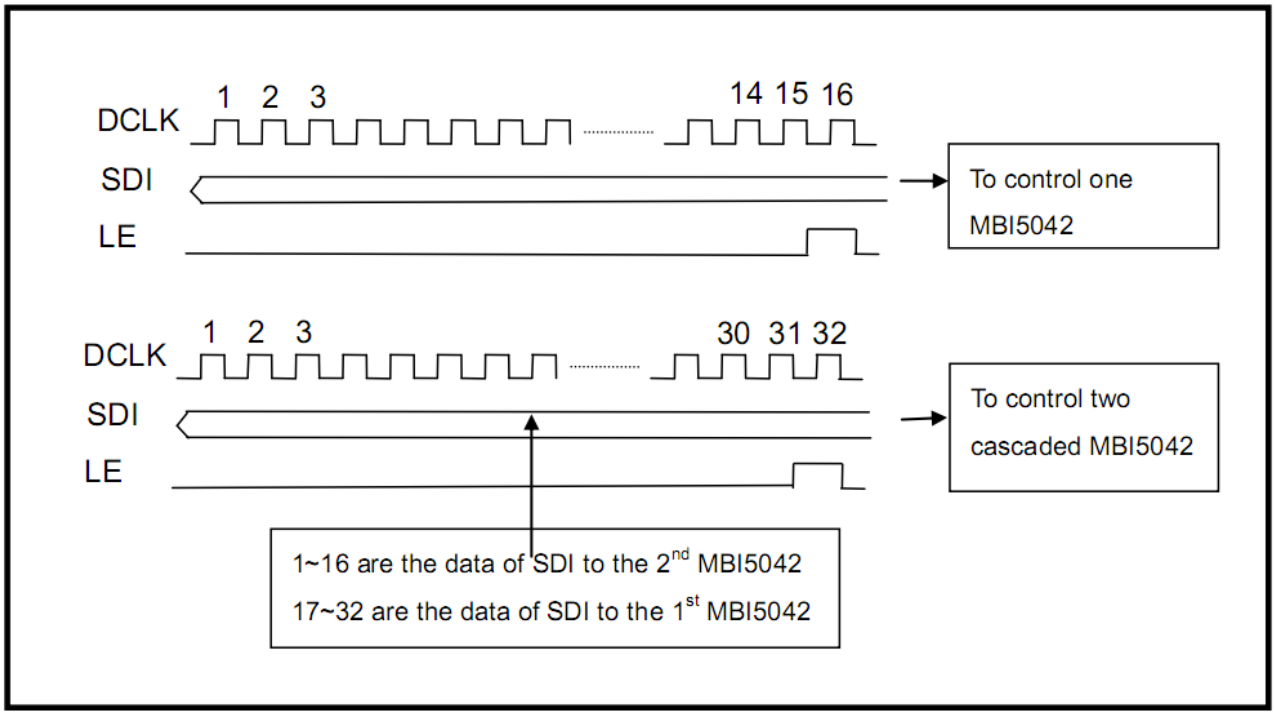

Figure 7. The timing diagram of “data latch” command

Section 4: Read/Write Configuration Register

MBI5042 embedded a readable and writeable configuration register which can determine the operation mode. The configuration register includes PWM counting mode selection, current gain adjustment, and etc.

The following timing diagrams illustrate the command of configuration register.

The command of “Enable Write Configuration” is LE high asserted 15-DCLK rising edges, and it should be executed before writing configuration every time.

Note that all the commands of MBI5042 are triggered by the falling edge of LE. The 32 bits data, which is counted forward from the falling edge of LE, is the data written into configuration register.

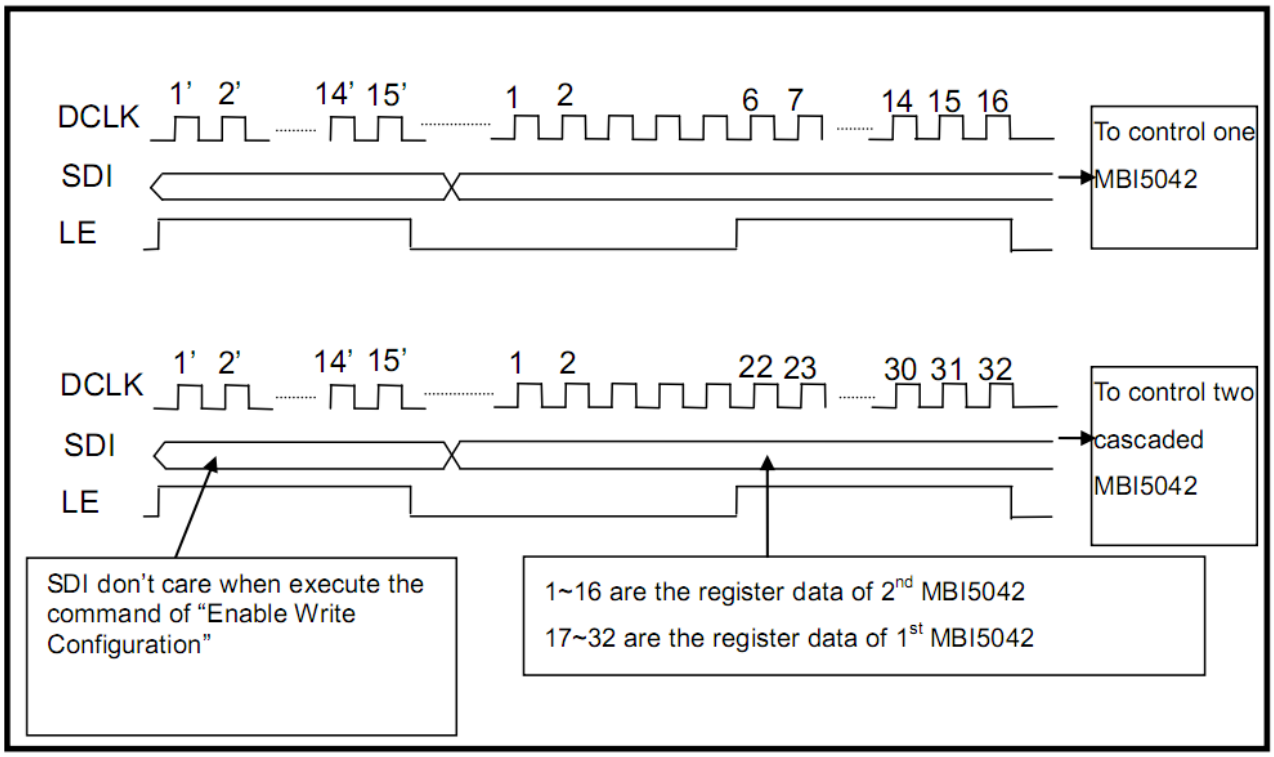

Figure 8. The timing diagram of write configuration command

Figure 9 shows the timing diagram of how to read the contents of the configuration register. The contents of the configuration register will be read from SDO after LE high asserted 5- DCLK rising edges.

At the falling edge of LE, the first data in configuration register will be sent out from SDO, and the other data will be read out with the rising edge of DCLK. The read out sequence of configuration register is from MSB (bit F) to LSB (bit 0). For example, if two MBI5042 are in cascaded, the read out sequence is from the configuration register of 2nd MBI5042 to 1st. During the command of “Read Configuration”, the SDI data means nothing.

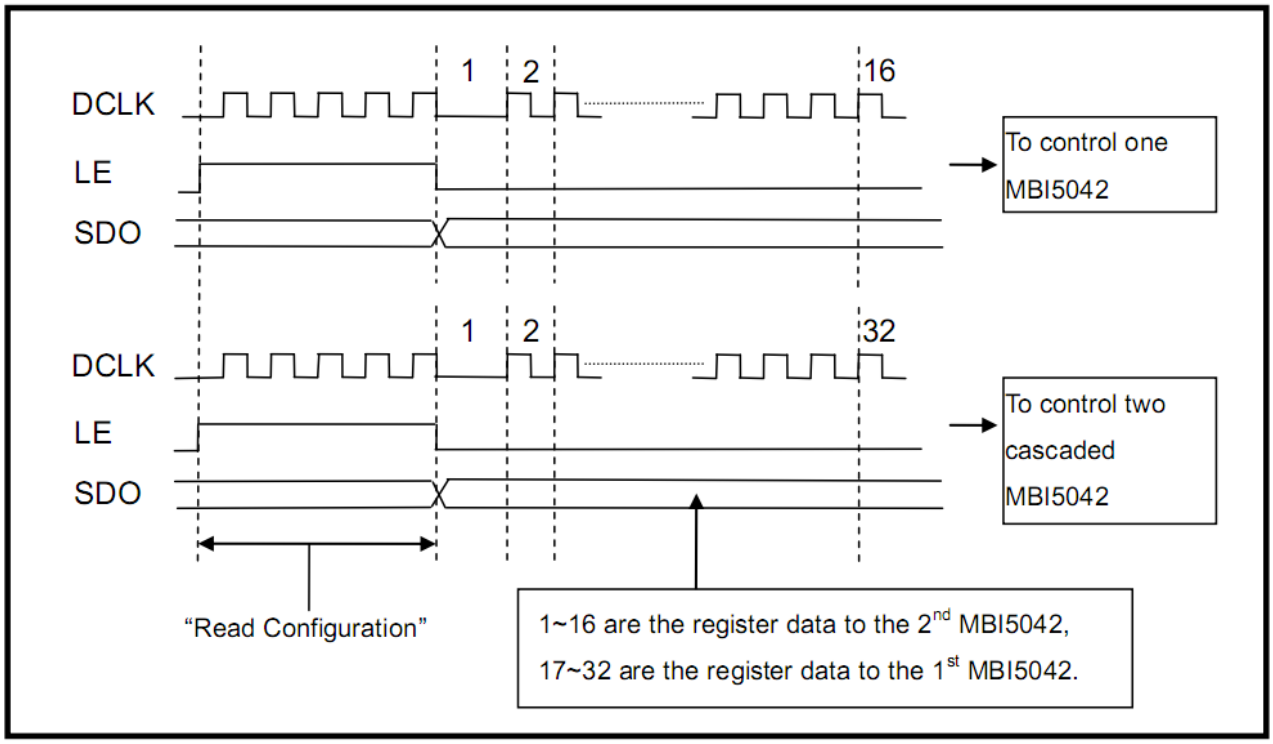

Figure 9. The timing waveform of “Read-Configuration”

Section 5: GCLK Rising/Falling Edge Trigger

MBI5042 provides a feature of GCLK rising/falling edge trigger. It can realize higher refresh rate at lower GCLK frequency and furthermore the lower EMI impact. In rising/falling edge trigger mode, a 16-bit PWM cycle can be accomplished in 32768 GCLK counts. A notice must be taken, due to the limitations of rise and fall times of output current. The duty cycle of GCLK must be keep at 50% in rising/falling edge trigger mode. The maximum frequency in rising/falling edge trigger mode is 16.5MHz to get consistency output.

Section 6: Refresh Rate and Pulse Width Calculation

With Scrambled-PWM (S-PWM) technology, MBI5042 enhances pulse width modulation by scrambling the “on” time into several “on” periods. Thus the technology increases the visual refresh rate. The following formulas can get the data refresh rate and pulse width in different image data (SDI).

Data refresh rate is (GCLK frequency/65536) X 64

Pulse width is (1/GCLK frequency) X (SDI data/64)

Minimum pulse width is (1/GCLK frequency)

Note that the calculation of refresh rate is suitable for the SDI data whose data length is larger than 64. Since the counting mode of MBI5042 is 10 bits+6 bits (The detail information please refers to page 11 of MBI5042 datasheet, The PWM Counting Mode), and the refresh rate is decided by the MSB. Therefore the data length of SDI must be larger than 64 bits, the basic refresh rate can be defined, as figure 10 shows. The minimum pulse width means the minimum on time of output channel.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

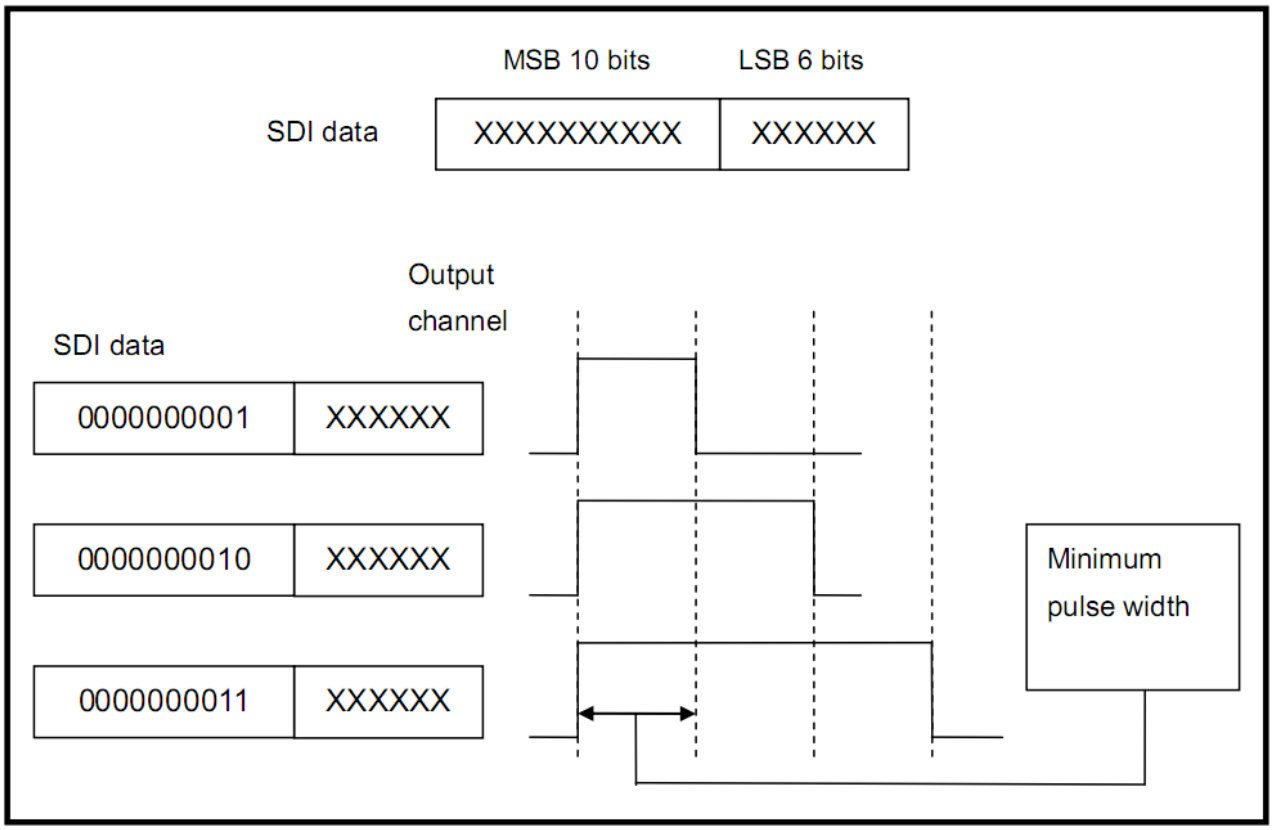

Figure 10. Schematic of SDI data and output channel's pulse width

Section 7: Synchronization for PWM counting

After executing the global latch command, the new data will be outputted immediately; even image data hasn't completed transmission. Figure 11 shows the schematic.

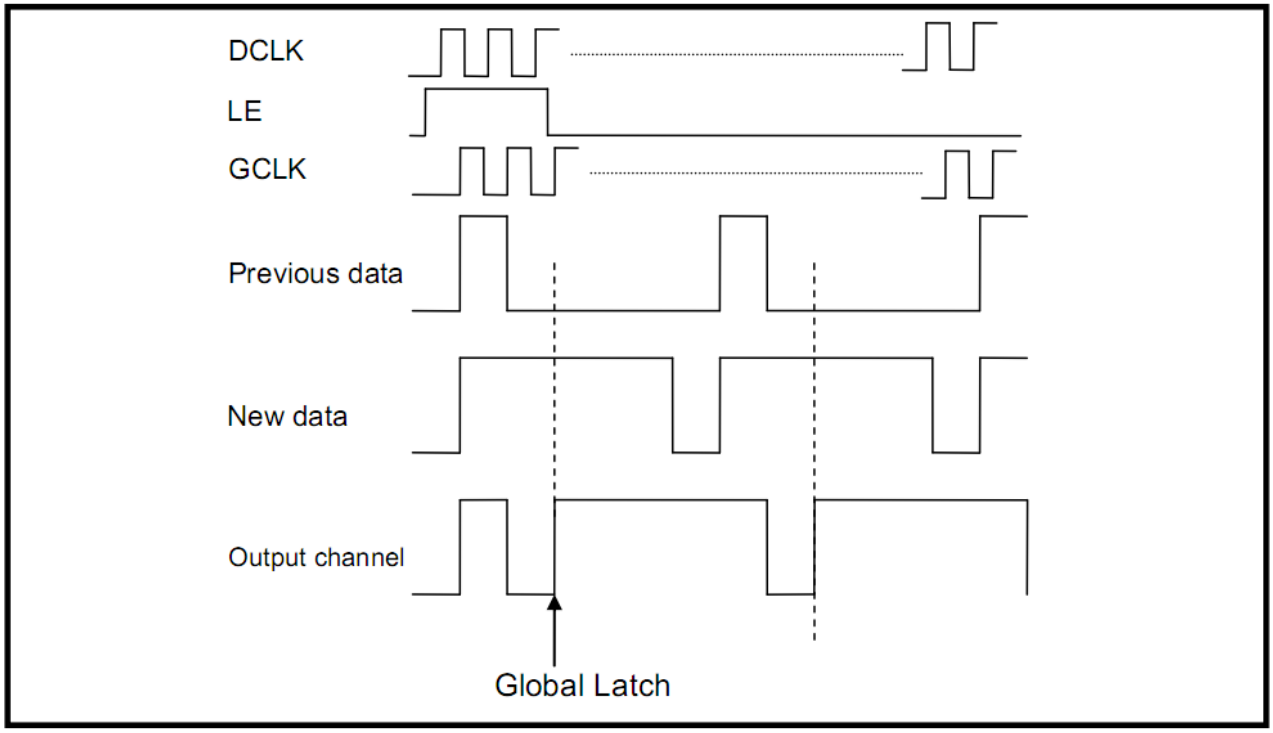

Figure 11. Schematic of synchronization mode

The advantage of synchronization mode is to update the next image data immediately. The disadvantage is system controller needs to synchronize the GCLK counter precisely, otherwise, when update the next image data, the turn-on time of output channel will exceed the expected time, as figure 12 shows.

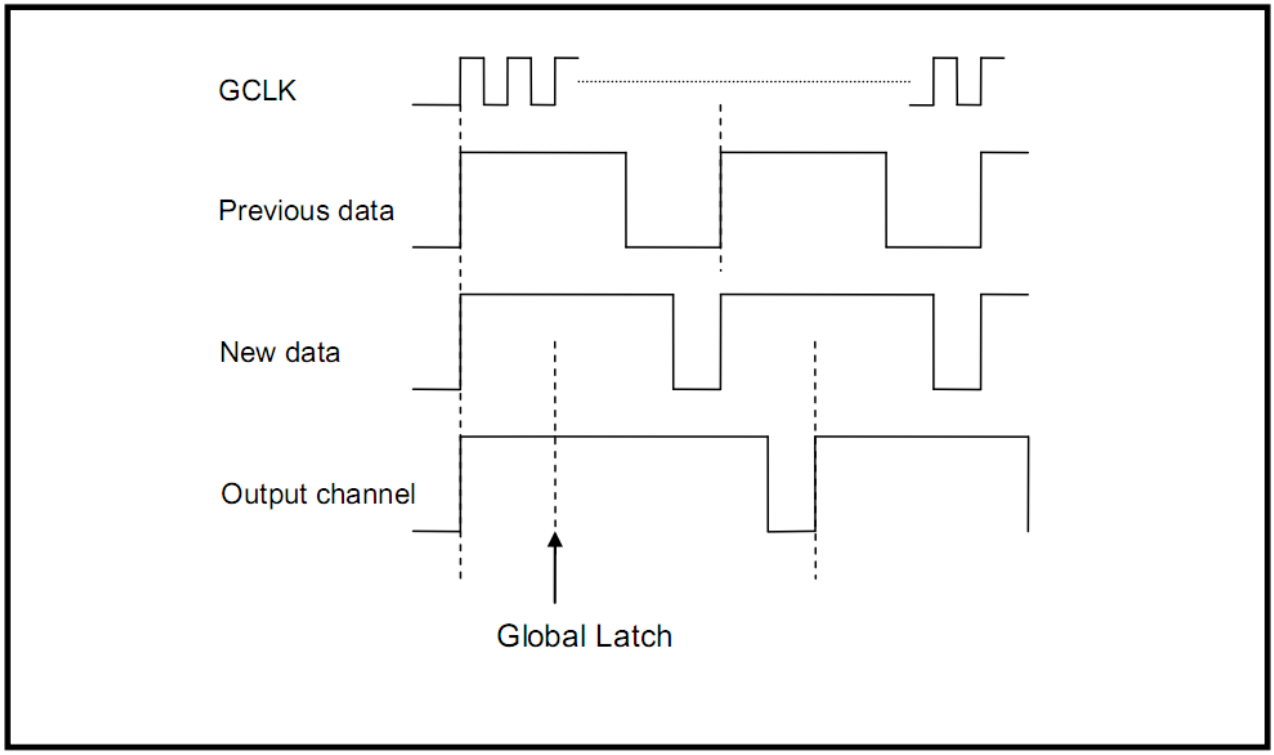

Figure 12. Potential question in synchronization mode

Section 8: Current Gain Adjustment

MBI5042 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, it should be controlled in the output current range of MBI5042; otherwise, the over designed output current can't be guaranteed.

The bit 9 to bit 4 in configuration register is used to set the current gain, and the defaulted gain code is 6'b101011.

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0				
Default	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0
							← 6-bit Current Adjustment →									

Figure 13 shows the relationship of current gain and gain code. The bit 9 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

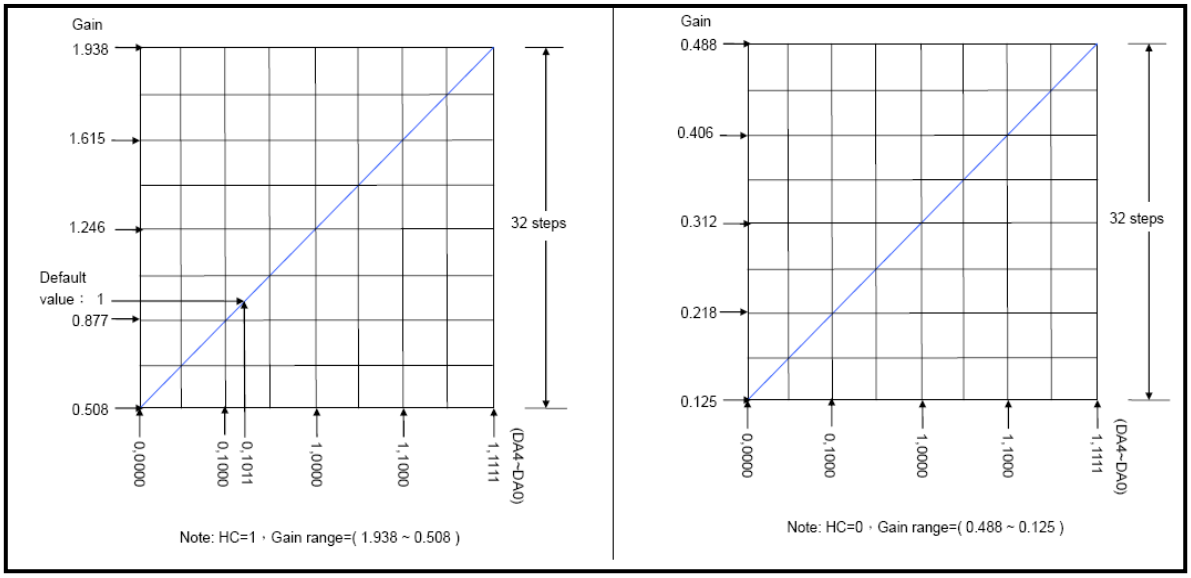

Figure 13. The relationship of current gain and gain code

The R_{ext} can be calculated by following equation

$$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 23.0 \quad \text{.....(4)}$$

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

$$HC=1,\ D=(65xG-33)/3 \quad \text{.....(5)}$$

$$HC=0,\ D=(256xG-32)/3 \quad \text{.....(6)}$$

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Example 1

If I_{OUT} =20mA and G=1, then the gain code is

Step 1: From (4), the R_{ext} = [(0.61 × 1) / 20mA] × 23 = 701.5Ω. From figure 13, G=1 in the high gain region, that means the HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary, D=01011, therefore DA[8:4]= 01011.

The 6 bits (bit 9~bit 4) of the configuration register are 6'b101011.

Example 2

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 30mA, then

Step 1: G= 30mA /20mA =1.5 (HC=1).

Step 2: From (5), D= (65x1.5-33)/3=21.5≒ 22.

Step 3: Convert D into binary, D=01011, therefore DA[8:4]= 5'b10110.

Step 4: The adjusted gain code is 6'b110110.

Example 3

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 5mA, then

Step 1: G= 5mA /20mA =0.25 (HC=0).

Step 2: From (6), D= (256x0.25-32)/3=10.67≒ 11.

Step 3: Convert D into binary, D=01011, therefore DA[8:4]= 5'b01011.

Step 4: The adjusted gain code is 6'b001011.

Figure 14 is the relationship of output current and gain data under V_{DD}=5.0V and R_{ext}=700Ω. The defaulted current gain, G =1, is corresponding to 20.6mA.

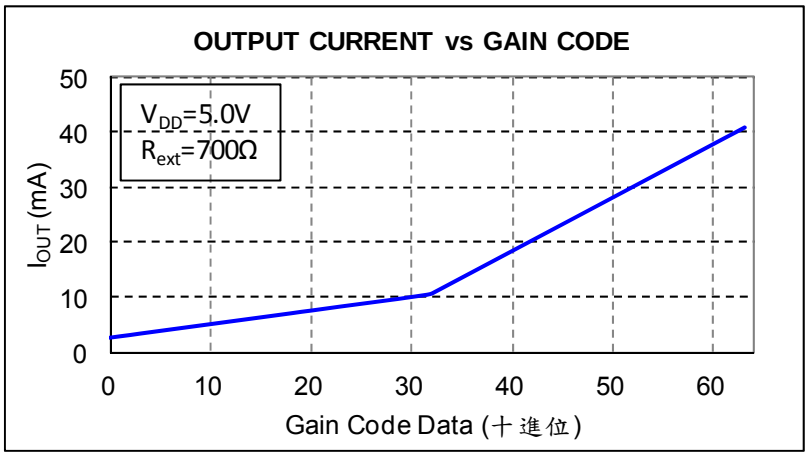

Figure 14. The relationship of current gain and code data under V_{DD}=5.0V and R_{ext}=700Ω.

Section 9: Time-multiplexing Application

MBI5042 can be applied in time-multiplexing application. Each MBI5042 needs 265 bits data to fill in 16 output channels, user should pay more attention on data refresh rate; otherwise the insufficient data refresh rate will affect the image performance in LED display. The detail description is shown as below sections.

Figure 15 shows the schematic of time-multiplexing structure in LED display.

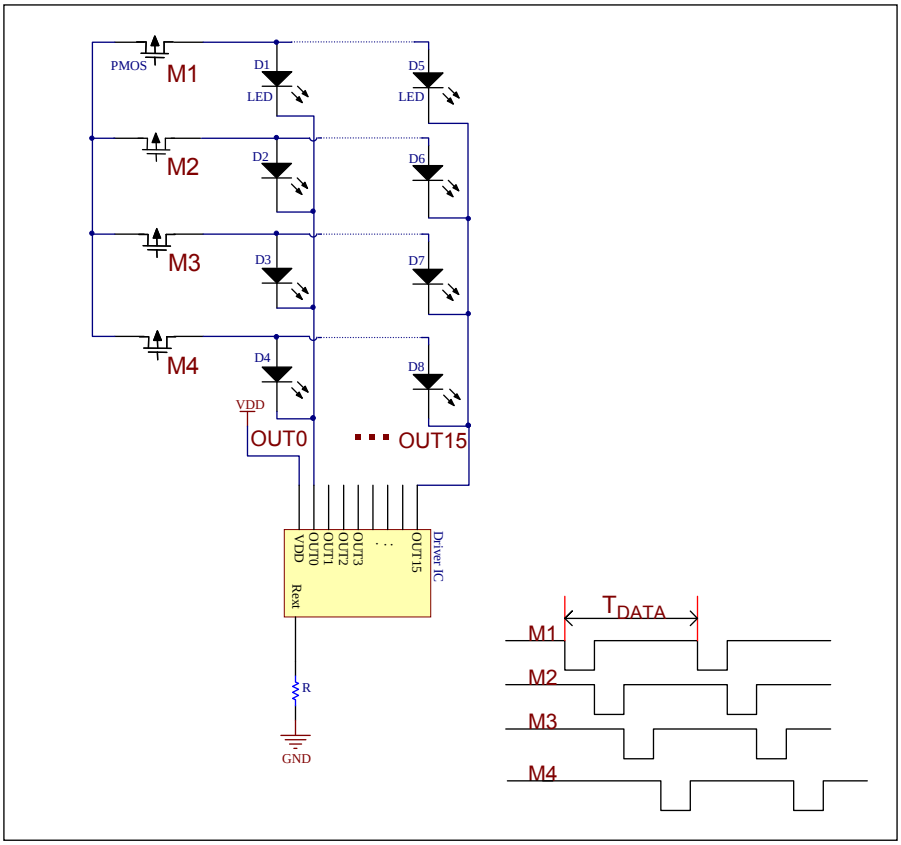

Figure 15. Schematic of multiplexing type LED board with MBI5042

Due to MBI5042 embedded a PWM grayscale counter, two issues should be taken in time-multiplexing application.

1. Can the speed of PWM counter meet the data refresh rate?

If the speed of PWM counter is slower than that of data refresh rate, the output data of each channel can't complete output, and that also means the function of PWM grayscale control is invalid. The following equation can be used to define the relationship.

$$F_{Time} = F_{GCLK} / 2^{Grayscale} / F_{DATA}$$
$$F_{Time} \geq 1$$

where

F_{GCLK}: GCLK frequency

F_{DATA}: Data refresh rate, (=1/T_{DATA}; T_{DATA} is the period of data update, referred the figure 15).

Grayscale: 16 bits grayscale

Let's take an example to explain this equation. The PWM grayscale counter is 16 bits, data refresh rate is 60Hz/second, and GCLK frequency 33MHz, then the F_{Time} is

$$F_{Time}= (33x10^6)/2^{16}/60=8.39$$

The calculation result is 8, and that means the GCLK counter can count 8 times in each data refresh; in other words, it only can be used in 1/8 duty of time multiplexing application. The frequency of GCLK is also an important factor in time multiplexing type application.

Table 1 shows the limitation of time-multiplexing application at GCLK is 33MHz.

Table 1. The cycle number of GCLK=33MHz in a period

Case	Bit number of gray scale control (bit)	Frame rate (Hz)	Duty cycle of multiplexing design	Cycle number of GCLK counter in a period T_{DATA}
1	16	60	1/8 duty	8
2	16	30	1/16 duty	16

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

2. Can all the data be delivered in the period of T_{DATA}?

The data quantity of each data refresh is huge for the PWM grayscale control IC. That's take an example of MBI5042 is employed in time multiplexing-type application, as figure 15 shows. Since the MOSFETs (M1~M4) will alternate turn on in turn, if the MOSFET turns off before data complete transmission, the grayscale data will be interrupted. The amount of cascaded MBI5042 is also an important factor to affect the data refresh rate. The amount limitation of cascaded MBI5042s can be calculated by following equation

$$N = (F_{DCLK} \times Duty) / (256 \times F_{DATA})$$

where

N: The amount of cascade MBI5042

F_{DCLK}: Frequency of serial data

F_{DATA}: Data refresh rate

Duty: Duty cycle of each LED

In time multiplexing application, the more scan lines, the less duty cycle of each LED can occupy, and also the less cascaded amount of MBI5042.

Take an example, if the frame rate is 60Hz/sec, DCLK frequency is 25MHz, and the duty cycle of multiplexing application is 1/8. The maximum cascaded amount of MBI5042 can be calculated

$$N = [(25 \times 10^6) \times (1/8)] / (256 \times 60) = 203.$$

The DCLK frequency and the duty cycle of each LED are the factors to determine the cascaded amount of MBI5042. Table 2 gives some examples to illustrate the relationship.

The above two issues have to be considered when using MBI5042 in time multiplexing application, then the display system can perform complete grayscale control.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Table 2. The maximum cascade numbers for MBI5042 at DCLK=25MHz

Case	Frame rate (Hz)	Duty cycle of T_{DATA}	Turned on time of every LED	The maximum cascade numbers of MBI5042
1	60	1/4 duty	4.165ms	406
2	60	1/8 duty	2.082ms	203
3	60	1/16 duty	1.041ms	101
4	30	1/4 duty	8.33ms	813
5	30	1/8 duty	4.165ms	406
6	30	1/16 duty	2.082ms	203

Scan Line Switching Notice

In time-multiplexing application, please follow the below steps and the figure 16 to switch scan lines.

Step 1. When the data of last scan line has completed, before switch to next scan line, please stop the signal of GCLK and maintain a duration of dead time. During the dead time, the output ports of decoder IC, which uses to control the scan line switching, also need to disable.

Step 2. Use the decoder IC to choose and set the next scan line, then enable the output ports of decoder IC.

Step 3. After complete above steps, please restart the signal of GCLK to recover the operation of MBI5042.

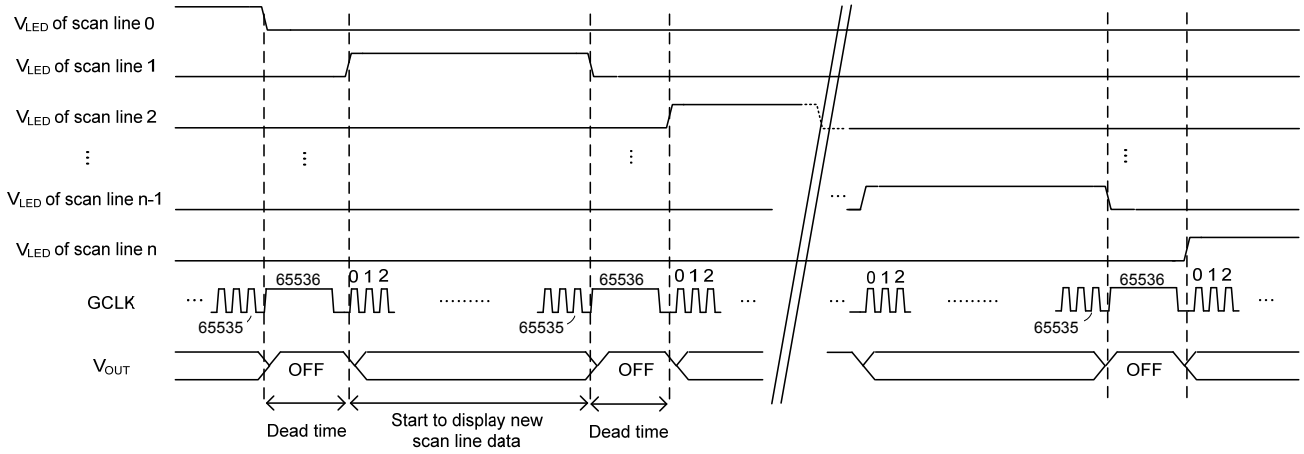

Figure 16. Scan line switching in time-multiplexing application

Section 10: How to Eliminate Ghost Problem

The phenomenon of unexpected LED in last scan line slightly turns on called “upper ghost problem”, and the unexpected LED in next scan line slightly turns on called “lower ghost problem”.

Figure 17 is an example of time-multiplexing application with n-scan lines. To avoid upper ghost problem, the discharge resistors, R1~Rn, between V_{LED} and GND are recommended. Typically, the resistance is 5.1KΩ and it can be adjusted based on the actual electric circuit situation.

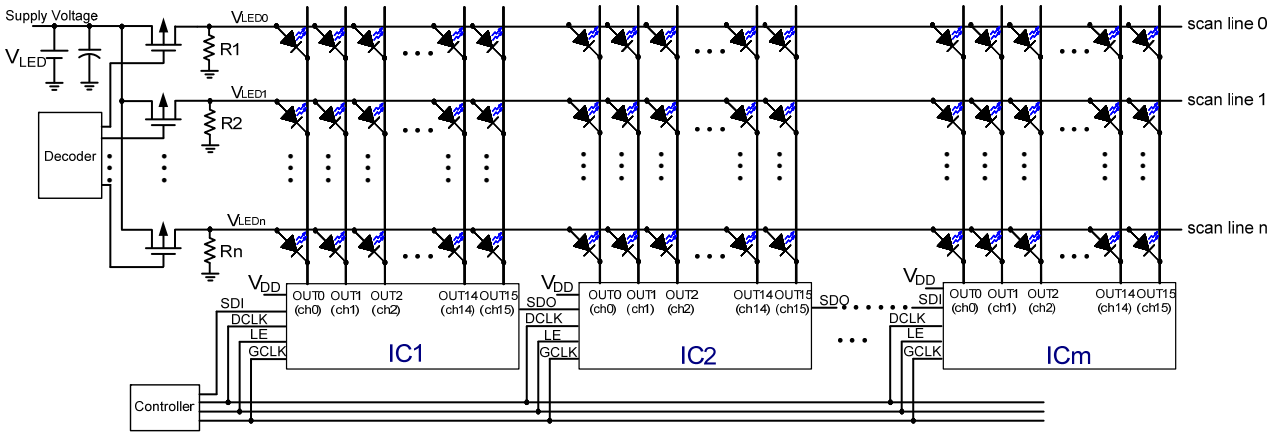

Figure 17. Time-multiplexing circuit diagram

The bit 0 of configuration register in MBI5042 is to enable the lower ghost elimination. As bit 0 is 1, the function of lower ghost elimination is enabled. Figure 18 illustrates the timing diagram of lower ghost elimination, in the dead time, a LE high asserts 3-DCLK rising edges is to execute the lower ghost elimination; and the duration of last LE falling edge to the next GCLK rising edge determines the running time of lower ghost elimination.

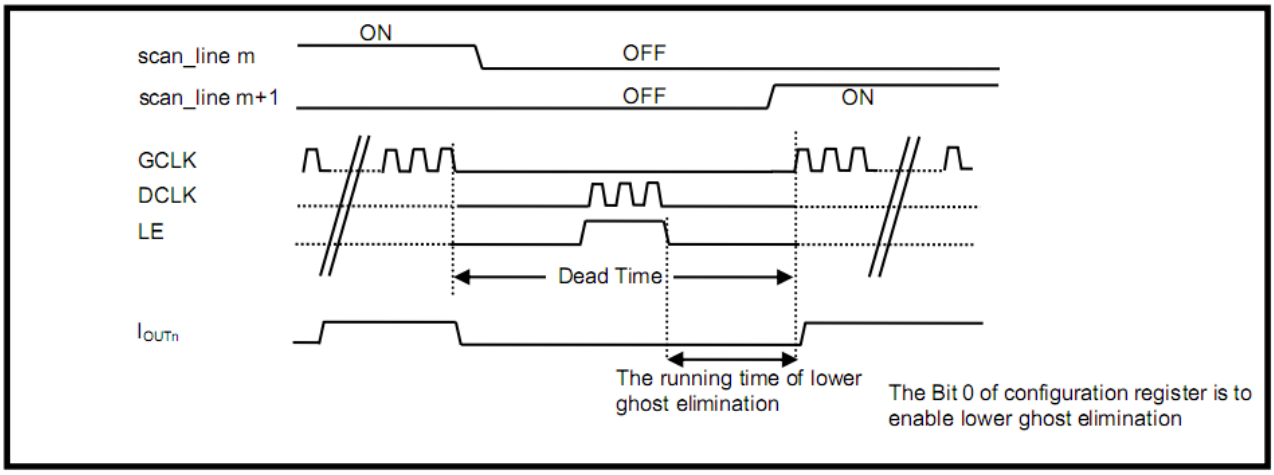

Figure 18. Timing diagram of lower ghost elimination

igure 19 shows an example of lateral scan with oblique angle, which has ghost problem, and figure 20 is the display board with the ghost elimination function.

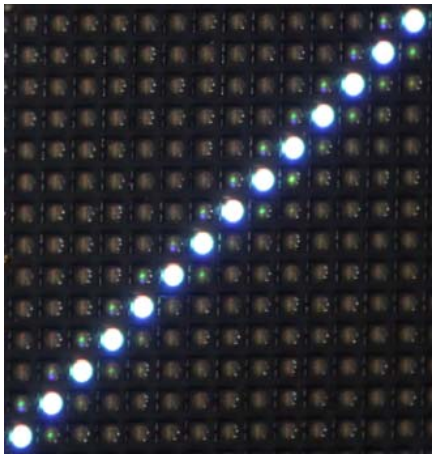

Figure 19. Display board with ghost problem

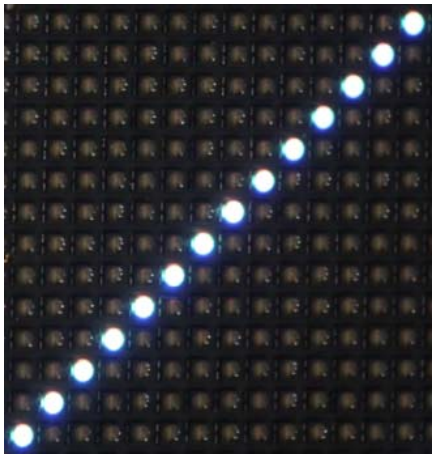

Figure 20. The display board with ghost elimination function

Section 11: Suggestions

1. Though the maximum frequency of GCLK is 33MHz in datasheet, GCLK frequency should be adjusted to optimize the display performance.
2. In the application of multi MBI5042 in cascaded, if the data quantity is too large to be delivered in a period, the distributed SDI input is recommended for signal quality. Also the buffer is necessary after long distance transmission. Please refer to “General Application Note” for the detail.
3. The detail circuit design and electrical characteristics please refer to “General Application Note”.
4. The thermal pad of MBI5042 doesn’t connect to internal GND. But consider the heat dissipation and environment optimized, short the thermal pad to GND pin is recommended. The details please refer to the “Application Note - How to Use Thermal Pad”.

Conclusion

MBI5042 is designed for LED video application, and the embedded SPWM technology enhances the visual refresh rate. MBI5042 also features the ghost elimination function to get great image quality in time-multiplexing application. This article is to provide a guideline for designer on how to use MBI5042.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw